

### **REMARKS**

This paper responds to the Office Action mailed on August 8, 2006. Claims 1-11 and 22-26 are pending in this application.

#### **§102 Rejection of the Claims**

Claims 1, 3-5, 7, and 10-11 were rejected under 35 USC § 102(b) as being anticipated by Lo et al. (U.S. 2003/0160312). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

*M.P.E.P. '2131*. To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states at pages 2-3 of the Office Action that Lo discloses

“Lo discloses a semiconducting device comprising (see Fig. 3): a substrate (102); a first die (104) attached to the substrate (102), the first die including active circuitry on an upper surface; a spacer (124; pg. 3, para 0035) covering the active circuitry on the upper surface (114) of the first die (104), the spacer (124) extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die (see Fig. 4); and a second die (106) stacked onto the spacer (124) and the first die (105).”

Applicant respectfully traverses these assertions because reference numeral 124 (cited by the Examiner as a spacer) refers to an adhesive bead 124 instead of a spacer.

Applicant also can not find any teaching or suggestion in the portions of Lo cited by the Examiner that the adhesive bead 124 extends from a first side of the first die 104 to an opposing second side of the first die 104. Applicant notes FIG. 4 of Lo shows that the opposing edges of the adhesive bead 124 do not extend to the opposing edges of the first die 112. In addition, Applicant can not find any description in the specification of Lo where one pair of opposing edges on the adhesive bead 124 extends from opposing edges of the first die 104 while the other

pair of opposing edges of the adhesive bead 124 extends near the other opposing edges of the first die 104.

Therefore, Lo does not appear to teach or suggest a semiconducting device that includes “the spacer extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die” as recited in claim 1. Claims 3-5 and 7-11 depend from claim 1, and are patentable over Lo for the reasons argued above, plus the elements in the claims.

The Examiner further states at page 3 of the Office Action that:

“Lo discloses wherein the spacer (124) includes at least one section that extends to the third side of the first die (104) such that the active circuitry is only partially exposed near the third side of the first die (104) (claim 3) and wherein the spacer (124) includes at least one section that extends to the fourth side of the first die (104) such that the active circuitry is only partially exposed near the fourth side of the first die (claim 4) (see Fig. 4).”

Applicant respectfully traverses these assertions because Applicant respectfully submits that the FIGS. and specification of Lo do not teach or suggest that any portion of any of the opposing edges of the adhesive bead 124 extend to any of the edges on the first die 104. Therefore, Lo does not appear to teach or suggest a semiconducting device that includes (i) “wherein the spacer includes at least one section that extends to the third side of the first die such that the active circuitry is only partially exposed near the third side of the first die” as recited in claim 4; or (ii) “wherein the spacer includes at least one section that extends to the fourth side of the first die such that the active circuitry is only partially exposed near the fourth side of the first die” as recited in claim 5.

Reconsideration and allowance of claims 1, 3-5 and 7-11 are respectfully requested.

#### First §103 Rejection of the Claims

Claims 1, 3-5, and 7-11 were rejected under 35 USC § 103(a) as being unpatentable over Thomas et al. (U.S. 2005/0194674). To sustain a rejection under 35 U.S.C. 103, references must be cited that teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)). In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves

would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02.

The Examiner states at page 4 of the Office Action that Thomas discloses

“a semiconducting device comprising (see Fig. 1): a substrate (110); a first die (112) attached to the substrate (110), the first die including active circuitry on an upper surface; a spacer (122) covering the active circuitry on the upper surface (116) of the first die (112), the spacer (122) extending from a first side of the first die to an opposing second side of the first die and a second die (114) stacked onto the spacer (122) and the first die (112).”

Applicant respectfully traverses these assertions as Applicant can not find any teaching or suggestion in the portions of Thomas cited by the Examiner that the spacer 122 extends from a first side of the first die 112 to an opposing second side of the first die 112. Applicant notes the FIGS. of Thomas only show two opposing edges of the spacer 122 that extend near opposing edges of the first die 112 without any views as to the other edges of the spacer 122 relative to the other opposing edges of the first die 112. In addition, Applicant can not find any description in the specification of Thomas where one pair of opposing edges on the spacer 122 extends from opposing edges of the first die 112 while the other opposing edges on the spacer 122 extend near the other opposing edges of the first die 112.

Therefore, Thomas does not appear to teach or suggest a semiconducting device that includes “the spacer extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die” as recited in claim 1. Claims 3-5 and 7-11 depend from claim 1, and are patentable over Thomas for the reasons argued above, plus the elements in the claims.

The Examiner further states at page 4 of the Office Action that “Thomas fails to specifically disclose extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die.” Applicant respectfully traverses these assertions because the FIGS. of Thomas only show two opposing edges of the spacer 122 that extend near opposing edges of the first die 112. Applicant

respectfully submits that there is no description in the specification of Thomas where one pair of opposing edges on the spacer 122 extends from opposing edges of the first die 112.

The Examiner further states at page 4 of the Office Action that

“It is well known in the art that a quad package would have all four sides of the active circuitry exposed. Although Thomas discloses only two sides of the active circuitry being exposed, it would have been obvious to one skilled in the art at the time of the invention for Thomas to have all four sides exposed.”

Applicant respectfully agrees with this assertion as acknowledged in the Background of the Invention section of Applicant’s specification. Applicant respectfully submits that what the cited references do not describe is one pair of opposing edges on the spacer extending from opposing edges of the first die while the other opposing edges on the spacer extend near the other opposing edges of the first die.

The Examiner further states at page 5 of the Office Action that Thomas discloses

“Regarding claims 4 and 5, Thomas discloses wherein the spacer (122) includes at least one section that extends to the third side of the first die (112) such that the active circuitry is only partially exposed near the third side of the first die (112) (claim 3) and wherein the spacer (122) includes at least one section that extends to the fourth side of the first die (112) such that the active circuitry is only partially exposed near the fourth side of the first die (claim 4) (see Fig. 1).”

Applicant respectfully traverses these assertions because Applicant respectfully submits that the FIGS. of Thomas only show two opposing edges of the spacer 122 that extend near opposing edges of the first die 112 without any illustration (or description in the specification) that at least a portion of either of the illustrated opposing edges of the spacer 122 extends to either edge of the first die 112.

Therefore, Thomas does not appear to teach or suggest a semiconducting device that includes (i) “wherein the spacer includes at least one section that extends to the third side of the first die such that the active circuitry is only partially exposed near the third side of the first die” as recited in claim 4; or (ii) “wherein the spacer includes at least one section that extends to the fourth side of the first die such that the active circuitry is only partially exposed near the fourth side of the first die” as recited in claim 5.

Reconsideration and allowance of claims 1, 3-5 and 7-11 are respectfully requested.

*Second §103 Rejection of the Claims*

Claim 2 was rejected under 35 USC § 103(a) as being unpatentable over Thomas et al. (U.S. 2005/0194674) in view of Katagiri et al. (U.S. 2002/0185744). As part of making the rejection, the Examiner states at page 5 of the Office Action that “Thomas discloses all claim limitations in claim 1 above . . .”

Applicant respectfully traverses this assertion. As discussed above, Thomas does not teach or suggest “the spacer extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die” as recited in claim 1. Applicant similarly can not find in Katagiri a spacer as recited in claim 1.

Claim 2 depends from claim 1 such that claim 2 incorporates all of the limitations of claim 1. Therefore, claim 2 is allowable for the reasons provided above with regard to claim 1.

The Examiner further states at pages 6 of the Office Action that

“It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the die of Katagiri with the teachings of Thomas because of advantages such as smaller size, lighter weight, a far lower power consumption and long life expectancy.”

Applicant respectfully traverses this assertion and notes that the statement does not appear to be supported by the references. In addition, the cited references do not appear to teach or suggest a spacer as recited in claim 1.

Reconsideration and allowance of claim 2 are respectfully requested.

*Third §103 Rejection of the Claims*

Claim 6 was rejected under 35 USC § 103(a) as being unpatentable over Thomas et al. (U.S. 2005/0194674) in view of Williams et al. (U.S. 4,910,643). As part of making the rejection, the Examiner states at page 6 of the Office Action that “Thomas discloses all claim limitations in claim 1 above . . .”

Applicant respectfully traverses this assertion. As discussed above, Thomas does not teach or suggest “the spacer extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the

first die such that the active circuitry is exposed near the third and fourth sides of the first die” as recited in claim 1. Applicant similarly can not find in Williams a spacer as recited in claim 1.

Claim 6 depends from claim 1 such that claim 6 incorporates all of the limitations of claim 1. Therefore, claim 6 is allowable for the reasons provided above with regard to claim 1.

The Examiner further states at page 6 of the Office Action that

“One would have been so motivated to modify Thomas with the pads of Williams to produce a much more economical circuit but also allow the spacer to cover all but 1 mm of the die.”

Applicant respectfully traverses this assertion and notes that the statement does not appear to be supported by the references. In addition, the cited references do not appear to teach or suggest a spacer as recited in claim 1.

Reconsideration and allowance of claim 6 are respectfully requested.

#### Fourth §103 Rejection of the Claims

Claim 22 was rejected under 35 USC § 103(a) as being unpatentable over Thomas et al. (U.S. 2005/0194674) in view of Katagiri et al. (U.S. 2002/0185744) and in further view of He et al. (U.S. 2004/0039859). Applicant initially notes that claims 23, 24 and 26 also appear to be rejected based on the comments in the rejection. Confirmation that claims 23, 24 and 26 stand rejected is respectfully requested.

The Examiner states at pages 6-7 of the Office Action that Thomas discloses

“the spacer extending from a first side of the die to an opposing second side of the die and extending near a third side of the die and an opposing fourth side of the die such that the active circuitry is exposed near the third and fourth sides of the die (see Fig. 1).”

Applicant respectfully traverses these assertions because as discussed above with regard to claim 1, Applicant can not find any teaching or suggestion in the portions of Thomas cited by the Examiner that the spacer 122 extends from a first side of the first die to an opposing second side of the first die. Applicant again notes the FIGS. and specification of Thomas only show two opposing edges of the spacer 122 that extend near opposing edges of the first die 112 without any views or description relating to the other edges of the spacer 122 relative to the other

opposing edges of the first die 112. Applicant similarly can not find in Katagiri or He a spacer as recited in claim 1.

Therefore, the cited combination does not appear to teach or suggest a semiconducting device that includes “the spacer extending from a first side of the flash memory to an opposing second side of the flash memory and extending near a third side of the flash memory and an opposing fourth side of the flash memory such that the active circuitry is exposed near the third and fourth sides of the flash memory” as recited in claim 22. Claims 23, 24 and 26 depend from claim 22, and are patentable over the cited combination for the reasons argued above, plus the elements in the claims.

The Examiner further states at page 7 of the Office Action that:

“Regarding claims 23-24, the prior art of Thomas, Katagiri and He teach all claim limitations as described above. Furthermore, Thomas and Katagiri disclose wherein the spacer includes at least one section that extends to the third side of the flash memory such that the active circuitry is only partially exposed near the third side of the flash memory (claim 23) and wherein the spacer includes at least one section that extends to the fourth side of the flash memory such that the active circuitry is only partially exposed near the fourth side of the flash memory (claim 24) (see Fig. 1-Thomas, para. 0069-Katagiri).”

Applicant also respectfully traverses these assertions because as discussed above with regard to claims 4 and 5, Applicant respectfully submits that the FIGS. of Thomas only show two opposing edges of the spacer 122 that extend near opposing edges of the first die 112 without any illustration (or description in the specification) that a portion of either of the illustrated opposing edges of the spacer 122 extends to either opposing edge of the first die 112.

Therefore, the cited combination does not appear to teach or suggest a semiconducting device that includes (i) “wherein the spacer includes at least one section that extends to the third side of the flash memory such that the active circuitry is only partially exposed near the third side of the flash memory” as recited in claim 23; or (ii) “wherein the spacer includes at least one section that extends to the fourth side of the flash memory such that the active circuitry is only partially exposed near the fourth side of the flash memory” as recited in claim 24.

The Examiner further states at page 7 of the Office Action that

“One would have been so motivated to modify Thomas and Katagiri with the electronic system of He to incorporate all separate structures to produce a general-purpose electronic system.”

Applicant respectfully traverses this assertion and notes that the statement does not appear to be supported by the references. In addition, the cited references do not appear to teach or suggest a spacer as recited in claim 22.

Reconsideration and allowance of claims 22-24 and 26 are respectfully requested.

*Fifth §103 Rejection of the Claims*

Claim 25 was also rejected under 35 USC § 103(a) as being unpatentable over Thomas et al. in view of Katagiri et al., He et al. and further in view of Li et al. (U.S. 6,493,861). As part of making the rejection, the Examiner states at page 8 of the Office Action that “The prior art of Thomas, Katagiri and He teach all claim limitations as described above . . .”

Applicant respectfully traverses this assertion. As discussed above, the cited combination of Thomas, Katagiri and He does not teach or suggest “the spacer extending from a first side of the flash memory to an opposing second side of the flash memory and extending near a third side of the flash memory and an opposing fourth side of the flash memory such that the active circuitry is exposed near the third and fourth sides of the flash memory” as recited in claim 22. Applicant similarly can not find in Li a spacer as recited in claim 22.

Claim 25 depends from claim 22 such that claim 25 incorporates all of the limitations of claim 22. Therefore, claim 25 is allowable for the reasons provided above with regard to claim 22.

The Examiner further states at page 8 of the Office Action that

“One would have been so motivated to modify Thomas, Katagiri and He with the voltage source of Li that results in less voltage drop and a much more efficient power delivery system.”

Applicant respectfully traverses this assertion and notes that the statement does not appear to be supported by the references. In addition, the cited references do not appear to teach or suggest a spacer as recited in claim 22.

Reconsideration and allowance of claim 25 are respectfully requested.



Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((262) 646-7009) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCOTT R. SAHAIDA ET AL.

By their Representatives,  
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
Attorneys for Intel Corporation  
P.O. Box 2938  
Minneapolis, Minnesota 55402  
(262) 646-7009

By / Andrew Peret \_\_\_\_\_ /  
Andrew R. Peret  
Reg. No. 41,246